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TITLE: BUS CLOCK CONTROLLING APPARATUS AND METHOD

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BUS CLOCK CONTROLLING APPARATUS AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates generally to computers, and more specifically to an apparatus and method for optimizing bus clock speed in a computer.

2. Background of the Related Art

[2] In general, a computer such as a notebook computer can be supplied with its necessary electric energy by either an equipped battery or an AC power line. However, because battery capacity is limited, a notebook cannot be used for more than a few hours if its power is supplied from the equipped battery.

[3] Fig. 1 is a simplified block diagram of a related art notebook. The notebook of Fig. 1 has a CPU 11 conducting ordinary well-known operations and functions; a bridge controller 12 conducting both assistant operations of the CPU 11 and management of memories, a video port, a bus, etc.; a video processor 13 for processing video data and outputting the processed data for video presentation; and a clock generator 10 providing 100MHz clock 1 for the CPU 11 and the bridge controller 12, and a 66MHz clock 2 for the video processor 13.

[4] A PLL (Phase Lock Loop) circuit 110 is embedded in the CPU 11. The PLL circuit 110 multiplies the 100MHz clock 1 from the clock generator 10 differently based on a current power supplying mode. For example, the PLL circuit 110 multiplies the 100MHz clock

by six times to produce a 600MHz internal clock if an external AC power is supplying energy, and it multiplies the 100MHz clock by five times to produce a 500MHz clock if a battery is supplying electric energy.

[5] Since power consumption of a CPU is proportional to the speed of a clock driving the CPU, if a 500MHz internal clock is used in a battery supplying mode, processing speed is lowered and power dissipation is decreased in comparison to application of a 600MHz internal clock. Therefore, battery life is extended in a battery supplying mode.

[6] In addition, a clock throttling method is also used to reduce power consumption in a CPU. Fig. 2 shows a clock throttling method in which a clock source is periodically made inactive by a control signal 'STPCLK#'. Whenever the control signal 'STPCLK#', which is active LOW, is in active state, a CPU clock is deactivated, so that the CPU dissipates little power. As a result, average power consumption by the CPU is reduced. Therefore, power consumption reduction rate of a CPU can be regulated through adjustment of a duty cycle of the control signal 'STPCLK#'.

[7] In related art portable computers configured and operated as above, the performance of a CPU is decreased during a battery supplying mode to reduce power consumption. However, the related art portable computers described above have various disadvantages. A host bus 3 to which both the CPU 11 and the bridge controller 12 are connected is driven by a bus clock, whose speed is fixed and whose state is always active, regardless of the power supplying mode. As a result, all devices connected to the host bus 3 are

being driven at all times. Therefore, power saving in a battery supplying mode is less effective than if power was also managed for devices connected to the host bus 3.

[8] The above references are incorporated by reference herein where appropriate for appropriate teachings of additional or alternative details, features and/or technical background.

SUMMARY OF THE INVENTION

[9] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[10] Another object of the present invention is to provide an apparatus and method of throttling a clock of a host bus to reduce power consumption.

[11] Another object of the present invention is to provide an apparatus and method of throttling a clock of a host bus connected to a CPU and a bridge controller in a portable computer.

[12] Another object of the present invention is to provide an apparatus and method of throttling a clock of a host bus in a portable computer based on remaining battery capacity, CPU load or the like.

[13] Another object of the present invention is to provide an apparatus and method of throttling a clock of a host bus, which both a CPU and a bridge controller in a computer are connected to, based on a remaining battery capacity or load to the CPU, in order to reduce power consumption.

[14] In order to achieve at least the above objects in whole or in part, and in accordance with the purposes of the invention, as embodied and broadly described, there is provided a bus clock controlling method in a computer that includes setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a CPU and a controlling device, detecting a remaining battery capacity if a present power source is at least one battery, and adjusting the set throttle rate according to the detected remaining battery capacity.

[15] To further achieve a least the above objects in whole or in part, there is provided a bus clock controlling method in a computer that includes setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a CPU and a controlling device, detecting a present load of the CPU, and adjusting the set throttle rate in reverse proportion to the present CPU load.

[16] To further achieve a least the above objects in whole or in part, there is provided a computer that includes a CPU that processes, a first controller coupled to the CPU via a data bus, and configured to provide a throttled clock to the data bus according to a throttle rate, a clock generator coupled to the CPU and the first controller, and configured to generate a clock, a detector detecting a variable, wherein the variable is a remaining battery capacity or a load of the CPU, and a second controller coupled to receive the detected variable, configured to determine the throttle rate according to the detected variable, and further configured to output the throttle rate to the first controller.

[17] To further achieve a least the above objects in whole or in part, there is provided a bus clock controlling method in a computer that includes setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus to which both a CPU and a controlling device are connected, detecting a remaining battery capacity and a load of the CPU if a present power source is a battery, and adjusting the set throttle rate according to the detected remaining battery capacity and the CPU load.

[18] To further achieve a least the above objects in whole or in part, there is provided a bus clock controlling method in a portable computer that includes setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a controlling device and a selected one of a plurality of devices associated with the portable computer, detecting a condition of a prescribed criteria of the portable computer if a present power source is a battery, and adjusting the set throttle rate according to the detected condition, wherein the detected condition is within a range of values for the prescribed criteria.

[19] To further achieve a least the above objects in whole or in part, there is provided a bus clock controlling method in a computer that includes setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus to which both a controlling device and a peripheral device are connected, detecting one of a present load of the CPU and a remaining battery capacity, and adjusting the set throttle rate in reverse proportion to the detected one of the present CPU load and the remaining battery capacity.

[20] To further achieve a least the above objects in whole or in part, there is provided a computer that includes means for setting a throttle rate of a data bus clock to a predetermined

initial value, means for detecting at least one of a remaining battery capacity and a load of the CPU, and means for adjusting the throttle rate of the data bus clock based on at least one of the detected remaining battery capacity and the detected load of the CPU.

[21] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[22] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[23] Fig. 1 is a simplified block diagram of a computer in the related art;

[24] Fig. 2 is a CPU clock signal diagram as provided in the related art;

[25] Fig. 3 is a block diagram that shows a computer including a bus clock controlling apparatus in accordance with a preferred embodiment of the invention;

[26] Fig. 4 is a diagram that shows a clock signal timing diagrams in accordance with a preferred embodiment of the invention;

[27] Fig. 5 is a logic diagram that shows a circuit embodying the throttle controller of Fig. 3 in accordance with a preferred embodiment of the invention;

[28] Fig. 6 is a diagram that shows a flow chart embodying a bus clock controlling method of a computer in accordance with a preferred embodiment of the invention;

[29] Fig. 7 is a diagram that shows a table of throttle rates and system performance for each range of remaining battery capacity according to a preferred embodiment of the invention; and

[30] Fig. 8 is a diagram that shows a flow chart embodying another bus clock controlling method of a computer in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[31] Fig. 3 is a block diagram of a computer in which a preferred embodiment of a bus clock controlling apparatus in accordance with the present invention is embedded. The portable computer of Fig. 3 may include a CPU 11, a bridge controller 22, and a clock generator 10 as described above and shown in Fig. 1.

[32] The clock generator 10 may provide the CPU 11 and the bridge controller 22 with a 100MHz clock 1, and the bridge controller 22 may include a throttle controller 220 throttling a clock for a host bus 103 to which the CPU 11 is also connected or connected together. As used herein, throttling a clock refers to causing a decrease in clock duty cycle.

[33] The computer with the preferred embodiment of a bus clock controlling apparatus of Fig. 3 may further have an embedded controller 23 including or consisting of a remaining battery capacity comparator 231 comparing a current remaining battery capacity with predetermined several references Ref_b1, Ref_b2,..., a CPU load comparator 232 and a host

clock throttler 230. The CPU load comparator 232 compares a current load to the CPU 11 with several predetermined references Ref_c1, Ref_c2,... . The host clock throttler 230 outputs a host clock control signal 'STP_HCLK' whose duty cycle preferably varies according to the comparison result of the remaining battery capacity comparator 231 or the CPU load comparator 232.

[34] The throttle controller 220 included in the bridge controller 22 may provide the 100MHz clock 1 from the clock generator 10 to the host bus 103 only while the host clock control signal 'STP_HCLK' from the host clock throttler 230 is inactive or low, as shown in Figs. 4 and 5. The examples depicted in Fig. 4 are for throttle rates of 50% and 25%, respectively. As used herein, a 25% throttle rate results in a 75% duty cycle for the host bus clock.

[35] The throttle controller 220 can be implemented with an inverter 50 and an AND gate 55 as shown in Fig. 5. However, the present invention is not intended to be so limited. In the logic circuit of Fig. 5, if the host clock control signal 'STP_HCLK' makes a transition to LOW, an input "$\overline{STP\_HCLK}$" to one terminal of the AND gate 55 becomes HIGH. The 100 MHz clock 1 is applied to the other input terminal of the AND gate 55. Thus, when "STP_HCLK" is LOW the 100 MHz clock 1 is output from the AND gate 55 and delivered to the host bus 103, to which the CPU 11 and the bridge controller 22 are connected.

[36] A remaining battery capacity detecting circuit (not shown in the figures), a CPU load detecting circuit (not shown in the figures), and a mode detecting circuit (also not shown in the figures) that detects whether an electric energy is supplied from an equipped battery or

an AC power source can all be implemented by well-known technology. Therefore, a detailed description of these features is omitted here.

[37] Fig. 6 is a flow chart embodying a first preferred embodiment of a method for throttling a host bus clock in accordance with the present invention. As shown in Fig. 6, the first preferred embodiment of a method for throttling a host bus clock is based on a remaining battery capacity of a computer. However, the present invention is not intended to be so limited. The throttle controller 220 included in the bridge controller 22 may set a throttle rate for the host bus clock to an initial value of zero (0%) upon computer boot-up in step S10. At this throttle rate, the computer performs fully.

[38] Next, in step S11, it is determined whether electric energy is supplied from an equipped battery or an external AC power source preferably using the embedded controller 23 or the like. If the power source is AC power, control jumps to step S20. If the battery is supplying the electric energy, a current Remaining Battery Capacity (RBC) may be compared with the several references Ref_b1, Ref_b2,... at the RBC comparator 231 in steps S12, S14, and S16. When the corresponding comparison is complete, the host clock throttler 230 may set the throttle rate to a new value in step S13, step S15, step S17 or step S18 according to the comparison result in steps S12, S14 and S16. The throttle rate may be set in reverse proportion to the RBC. As a result, the battery life and its operating time is extended when the RBC is small, even though the performance of the portable computer may be lowered.

[39] For example, if it is determined in step S12 that the RBC is above 75%, then the throttle rate may be set to 15% in step S13. If it is determined in step S14 that the RBC is in

range of 75% to 51%, the throttle rate may be set to 30% in step S15. If it is determined in step S16 that the RBC is in the range of 50% to 26%, then the throttle may be set to 45% in step S17. If it determined in step 16 that the RBC is 24% or lower, then the throttle rate may be set to 60% in step S18.

[40] From steps S13, S15, S17 and S18, control continues to step S19 where it is determined if a power source is AC power. If AC power is detected in step S19, then the throttle rate may be initialized in step S20. Otherwise, control returns from step S19 to step S12.

[41] Fig. 7 tabulates exemplary respective throttle rate and system performance for each range of remaining battery capacity. As shown in Fig. 7, the system performance may be lowered as the throttle rate is raised, namely, if the throttle rate is raised by T%, the system performance may be lowered by (100-T)%.

[42] During the time when the host clock is not provided, all devices that operate in synchronization with the host clock cannot conduct data exchange operations. Therefore, such devices do not dissipate the supplied power. Of course, system performance may be lowered.

[43] Fig. 8 is a flow chart embodying a second preferred embodiment of a method of throttling a host bus clock in accordance with the present invention. As shown in Fig. 8, the second preferred embodiment of a method of throttling a host bus clock is based on a load to a CPU of a computer. In the preferred embodiment of Fig. 8, the throttle rate for the host bus clock 1 may be set to an initial value, e.g., zero, at system booting in step S30. In this instance, all pulses of the 100MHz clock 1 from the clock generator 10 are used as the host bus clock and the computer operates at full performance.

[44] Next, it is determined in step S31 whether an electric energy is fed from an equipped battery or an external AC power source preferably using the embedded controller 23 or the like. If the battery is supplying the electric energy, a current CPU load may be compared in step S32 with a plurality of load references such as the load references Ref_c1, Ref_c2,... at the CPU load comparator 232.

[45] For example, if the comparison by the CPU load comparator 232 indicates that the current CPU load is above 90%, the host clock throttler 230 may maintain the initial throttle rate of 0% in step S33, and if the CPU load is below 90%, host clock throttle 230 may adjust the throttle rate in reverse proportion to the CPU load in step S34 in order to extend the battery life and its operating time, although the performance of the portable computer may be lowered. From steps S33 and S34, control continues to step S35.

[46] Alternatively, step S32 may be expanded into a series of CPU load comparisons that may result in a range of adjustments to host clock throttle in step S34. For example, if the current CPU load is determined to be in the range of 90% to 75% of full load in step S32, the throttle rate may be set to 15% in step S34 by adjusting duty ratio of the host clock control signal to 15%. As a result, 85% of the pulses of the 100MHz clock 1 from the clock generator 10 are provided for the host bus by the throttle controller 220. Likewise, if the current CPU load is in range of 75% to 50%, the throttle rate may be set to 30%; if CPU load is in the range of 50% to 25%, the throttle rate may be set to 45%; and if the CPU load is below 25%, the throttle rate may be set to 60%.

[47] From steps S33 and S34, control continues to step S35. If it is determined in step S35 that a power source is switched from a battery to an AC source after the throttle rate is adjusted as described, the throttle rate may be reset to 0% in step S36, as in step S30, in order to fully operate or maximize system performance.

[48] The second preferred embodiment of a method of throttling a host bus clock depicted in Fig. 8 is also applicable to an AC power supplying mode as well as battery supplying mode. It may be advantageous, for example, to conserve power even when the computer is not powered with a battery source.

[49] In the preferred embodiments according to the present invention, the host clock throttler 230 or the like may calculate the throttle rate based on the following equation (1) instead of selecting a condition-matching value among several predetermined throttle rates as described with reference to Figures 6-8 above.

$$TR\ (\text{Throttle Rate}) = MR - (MR \times X/Xmax) \quad \text{.....Eq. (1)}$$

where X is a variable of battery remaining capacity or CPU load, Xmax is maximum value of variable X, and MR is maximum or prescribed throttle rate.

[50] For example, if a battery is at 30% capacity and the maximum throttle rate is 60, then X may be 3, Xmax may be 10, and the throttle rate $TR = 60 - (60 \times 3/10) = 60 - 18 = 42\%$. In another preferred embodiment, X and Xmax may refer to CPU loads. However, the present invention is not intended to be so limited. The above-described throttle rate adjusting operations are preferably executed through a timer interrupt service routine that wakes up periodically, for example, every 100ms.

[51] The preferred embodiments are applied to the host bus to which a CPU and a bridge controller are connected. However, throttle rate adjusting operations and apparatus according to preferred embodiments of the present invention are also applicable to a PCI bus to which a bridge controller and one or more peripheral devices are connected.

[52] As described above, preferred embodiments of bus clock controlling apparatus and methods have various advantages. Preferred embodiments of host bus clock controlling apparatus and methods can adjust performance of devices connected to a data bus according to a remaining battery capacity or a CPU load by throttling a clock of the data bus. Thus, power consumption in a battery-powered computer system may be reduced, and battery life and operating time may be extended. Throttling based on CPU load may also conserve power in a AC-supplied computer.

[53] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.